Scalable charge pump design for the PLL

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1 Description of the circuit

The purpose of the charge pump is to be interfaced with a phase-frequency detector generating *up* and *down* signals. A charge pump is a controlled current source whose output is defined as follows:

$$I_{out} = \begin{cases} I_0, & up =' 1', dn =' 0' \\ -I_0, & up =' 0', dn =' 1', \\ 0, & otherwise \end{cases} \tag{1}$$

Since the charge pump is a current generator, the output voltage is an external parameter and is set to any value between 0 and Vdd, however, the nominal value of the output voltage is $Vdd/2$. The interval of V_{out} for which the charge pump operates properly (as described by (1)) is narrower than $[0, Vdd]$, as it will be seen later.

A typical structure of a charge pump is given in fig. 1.

2 CMOS implementation of the charge pump

The current sources and the switches are implemented with MOS transistors. The current sources are implemented with transistors having large L, in order to minimise g_{ds}. The switches are implemented by transistors with a miminium L but with a strengths (W/L ratio) greater than the current generation transistors.

The input signals of the charge pumps are named *upmos* and *dnmos*. Their relation with *up* and *dn* of eq. (1) is:

$$\begin{cases} dnmos = Vdd, upmos = Vdd, & if\ up =' 1', dn = 0 \\ dnmos = 0, upmos = 0, & if\ up =' 1', dn = 0 \\ dnmos = 0, upmos = Vdd, & otherwise \end{cases} \tag{2}$$

The current sources need to be biased. The bias circuit is proposed in fig. 2.

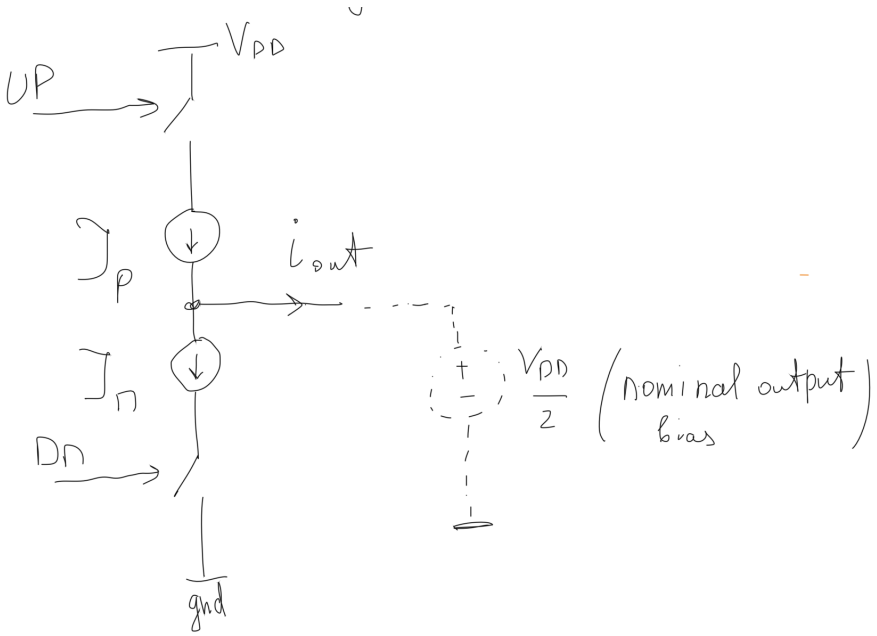

Figure 1: Functional structure of a charge pump

The bias circuit receives the reference current generated from the outside of the cell (e.g., is generated by a quad or by a bandgap generator).

In order to save power, the bias generators is based on current mirrors with a ratio $1 : K$, where K is the ratio between the output current of the charge pump I_0 and the reference current:

$$K = I_0/I_{ref} \tag{3}$$

The bias for the transistor $Mnsr$ is generated by the transistors $M1$ and $M11$, which are a downscaled by K replica of $Mnsr$ and $Mnsw$. The gate of the transistor $M11$ is biased by Vdd, since the gate of $Mnsw$ is biased by Vdd when dn is '1' (and $dnmos$ is Vdd). So we need to include an "always on" transistor $M11$ in this structure.

The transistors $M1$ and $M11$ generate a gate voltage V_{biasn} corresponding to the current $Iref$. This voltage is applied to a replica of $M1$ and $M11$, the transistors $M2$ and $M21$, which generate the same current as $Iref$. This current is applied to the transistors $M3$ and $M31$ which are a replica of $Mpsr$ and $Mpsw$, downscaled by K. The transistors $M3$ implements a MOS diode, and $M31$ is always on as its gate is always on the ground.

In this way, the transistors $M3$, $M31$, $M2$ and $M21$ form a downscaled version of the charge pump cell.

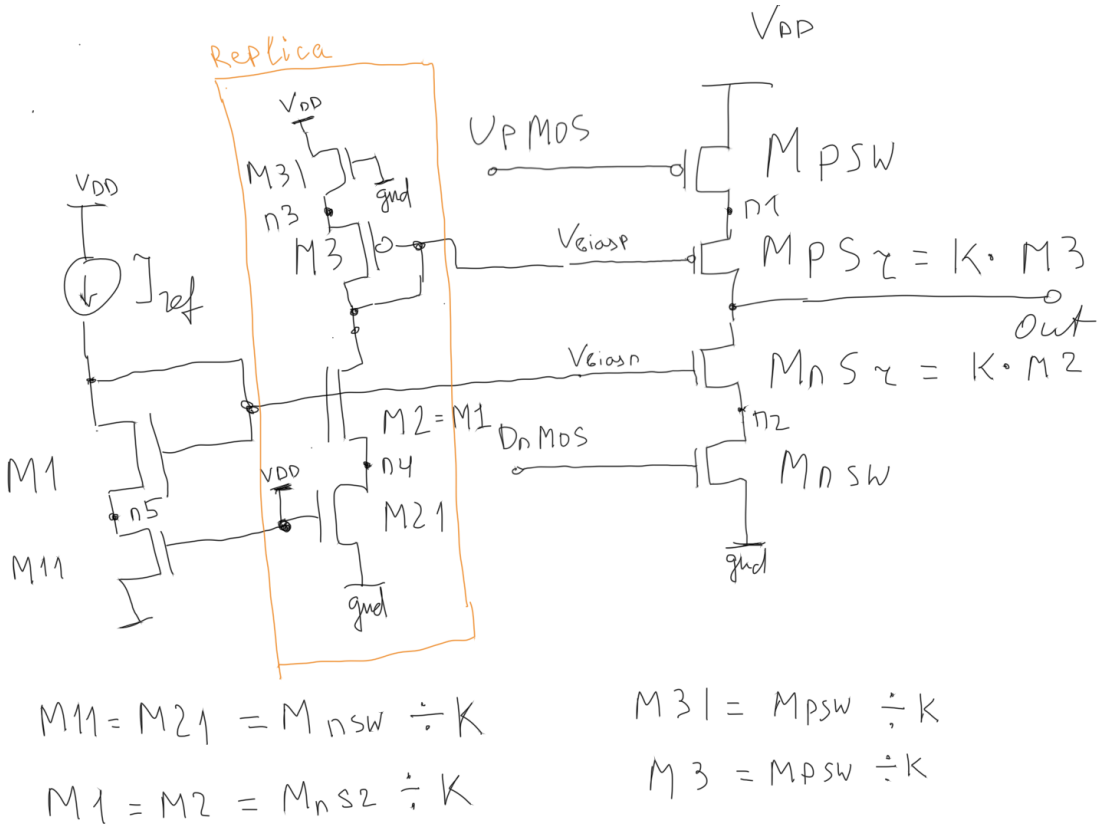

Figure 2: Schematic of the CMOS charge pump

M1	Lc	W1	M11	Ls	Wnsw1
M2	Lc	W1	M21	Ls	Wnsw1
M3	Lc	W3	M31	Ls	Wpsw1
Mnsr	Lc	Wnsr	Mnsw	Ls	Wnsw
Mpsr	Lc	Wpsr	Mpsw	Ls	Wpsw

Table 1: List of parameters of each transistor

3 Sizing algorithm

Input parameters:

- Ls: length of the switches, set to $Ls = Lmin$ (transistors $M11$, $M31$, $M21$, $Mpsw$, $Mnsw$)
- Lc: length of the current generators (transistors M1, M2, M3, Mnsr, Mpsr), set to $Lc = m \times Lmin$, where $m \geq 1$, min. recommended value is 3. A large L reduced g_{ds} of the current generators and makes the generated current less dependend on V_{out}.
- m: ratio between the lenght of the current generators (transistors M1, M2, M3, Mnsr, Mpsr) and the minimum lenght allowed by the technology, see the parameter Lc. Default (minimum recommended) value 3.
- K: the ratio between the output current I_0 and the reference current I_{ref}. Set by the user as a function of the available reference generator and the wanted output current.
- KSW: the ratio between the widths of the switch transistors $Mnsw$, $Mpsw$ and the current generation transitors $Mnsr$, $Mpsr$. The same is the ratio between the corresponding bias generation (replica) transistors.

  It is recommended to set this ratio to 1, maximum 3. Default $KSW = 1$.

The table 1 presents the list of the parameters of the transistors as they are named in the python generator.

1) Before sizing the cell, a calculation of a ratio between the width of $pMOS$ and $nMOS$ transistors of an equilibrated CMOS invertor need to be done (see the algorithm used in the generator of a VCO). This ratio is named n.

2) Transistor M1. Since typical current generated by the charge pumps are very low (max. hundreds of microamps), we can size the replica transistors with a minimum W. Hence, $W1 = Wmin$.

3) Transistor M11. This is the replica of the transistor used for the switch. Its width is KSW times greater than the width of $M1$. So $W_{M11} = Wnsw1 = KSW \times W1$.

4) Transistors $M21$ and $M2$: they are identical with the transistors $M11$ and $M1$.

5) Transistors $M31$ and $M3$: they have the same widths as the transistors $M21$ and $M2$ respectively, scaled by the factor n. So:

$W_{M31} = Wpsw1 = n \cdot Wnsw1$

and

$W_{M3} = W3 = n \cdot W1$

6) The sizing ends with the calculation of the widths of the transistors $Mpsd$, $Mpsr$, $Mnsr$ and $Mnsr$: they are the same as the width of the transistors $M31$, $M3$, $M2$, $M21$ but multiplied by K.

4 Improvement of the dynamic properties of the charge pump

Two simple adding improve dynamic behaviour of the charge pump.

The first concerns the stabilisation of the bias voltages, Vbiasn and Vbiasp, see fig. 2. This is done by connecting large capacitors between these nodes and the ground. The value of the capacitors is an order of magnitude above the capacitors of the transistors Mpsw, Mpsr, Mnsr and Mnsw. The capacitors should not be too large, otherwise it will be expensive (the area) and it will affect the transient time at the power-on.

The second concerns the filtering out of very short pulses at the inputs of the charge pump, which correspond to correction of small errors. Indeed, a short pulse upmos or dnmos means that a very small correction to the error must be done.

These modifications are presented in blue in fig. 3.

5 Test of the charge pump

The charge pump was tested in the DC mode by sweeping $V_{out} = 0...Vdd$ and by setting, subsequently the input voltage into one of two configurations :

- $upmos = dnmos = Vdd$ for the verification of the current generated by the $nMOS$ transistors,
- $upmos = dnmos = 0$ for the verification of the current generated by the $pMOS$ transistors,

Two plots are obtained, as in fig. 4.

On this characteristics it can be seen that the range of the current generation is when $V_{out} \in [V_{ds\ sat\ n}, Vdd - V_{ds\ sat\ p}]$

One can also see that in the nominal behaviour the current depends slightly on V_{out}. This is a parasitic effect due do a non-zero gds. This effect is reduced as the parameter Lc increases.

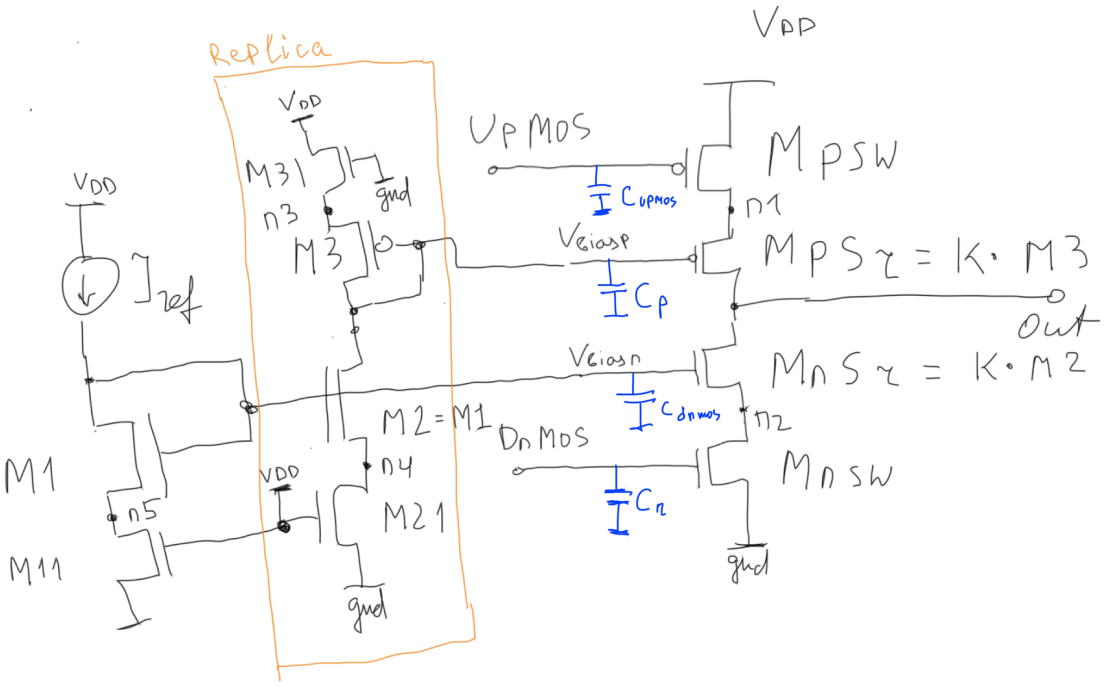

Figure 3: Schematic of the CMOS charge pump with added capacitors.

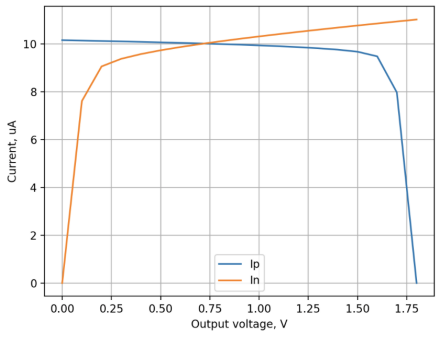

Figure 4: Example of characteristic obtained for the charge pump