

Scalable PLL design

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1 PLL architecture

The implemented PLL architecture is given on fig. 1. This is a PLL of type 3 containing three pure integrators in the open loop (capacitors C_1 and C_2 and the voltage controlled oscillator, VCO).

The linear model in the phase domain of the implemented PLL is given in fig. 2.

The VCO is a voltage-controlled oscillator. The frequency divider by N can be incorporated into the VCO if the frequencies are scaled by N , yielding the equivalent structure shown in the green frame in fig. 1. The useful output of the PLL is somewhere between the output of the real VCO (labeled $f_{ref} \times N$ in the figure) and the output of the divider. For instance, if a divider is a cascade of dividers such as $N = N_1 \cdot N_2 \cdot N_3$, the output of the PLL can be the output of any of the cascades yielding frequencies differently related to f_{ref} .

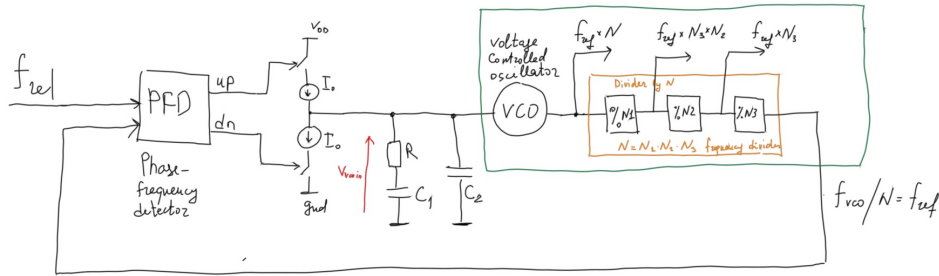


Figure 1: Structure of the designed PLL

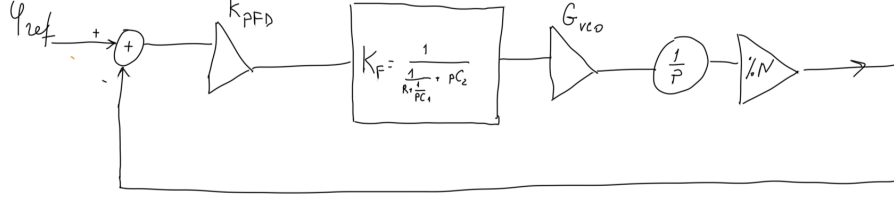


Figure 2: Linear model of the designed PLL

The open loop transfer function in the phase domain between the input (reference signal) and the output of the divider is given by:

$$H(p) = K_{pfd} \frac{1}{\frac{1}{\frac{1}{K_1 C_1} + p C_2}} \frac{G_{vco}}{p} \quad (1)$$

Here

$$G_{vco} = 2\pi K_{vco}/N, \quad (2)$$

is the gain of VCO in $rad \cdot Hz/V$, where K_{VCO} is the gain of the physical VCO, in Hz/V .

The closed loop transfer function is

$$K(p) = \frac{H(p)}{1 + H(p)} = \frac{K_{pfd} G_{VCO} (1 + C_1 p R)}{K_{pfd} G_{vco} + (C_1 + C_2) p^2 + C_1 K_{pfd} G_{vco} p R + C_1 C_2 p^3 R} \quad (3)$$

A PLL is a closed-loop regulation system. The input of a PLL is the phase of the reference clock signal, the output is the phase of the signal issued from the divider and generated by the VCO. Since the frequency of the source is constant, the input phase evolves linearly:

$$\phi_{ref} = \int 2\pi f_{ref} dt = 2\pi f_{ref} t + \phi_0 \quad (4)$$

The VCO, after a divider, must produce the same phase. The error is measured by the phase-frequency detector (PFD), and the output voltage of the PFD is proportional to the phase error. The loop filter (regulator) generates a command for the VCO so to adjust its phase. The input voltage of the VCO controls the frequency of the VCO, and hence, its phase, since the phase and the frequency are in a differential-integral relation.

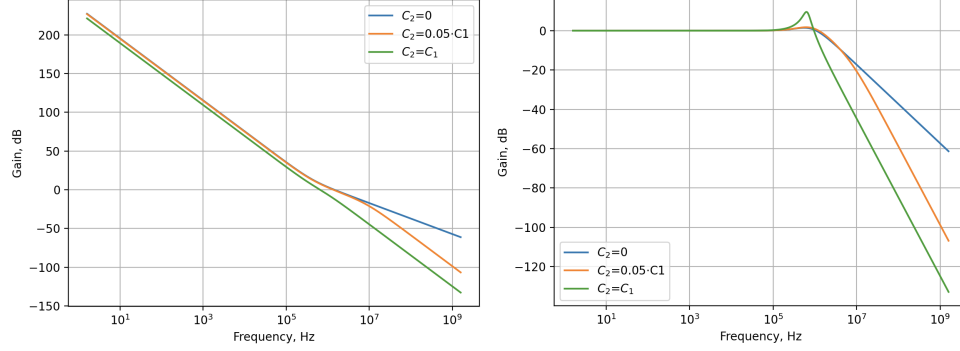


Figure 3: Influence of the capacitor C_2 on the frequency characteristics of the PLL: a) Open loop, b) Closed loop.

A proportional-integral (PI) corrector is the most used solutions for the PLLs.

When $C_2 = 0$, the network R_1C_1 implements a PI filter for the current generated by the charge pump. Indeed,

$$V_{out\ cp} = I_{out\ cp} \left(\frac{1}{C_1 p} + R \right) \quad (5)$$

Here $I_{out\ cp}$ is the average output current of the charge pump. The instantaneous current of the charge pump can take only three values ($+I_0$, $-I_0$ and 0). This current is, in fact, a PWM (Pulse Width Modulation) signal: only its average values codes the useful information about the phase error. Hence, one of the roles of the loop filter is the selection of the average current and filtering out the PWM ripples.

In order to improve the reduction of the PWM noise at high frequencies, a capacitor C_2 is added to the filter. It should be much smaller than the capacitor C_1 , otherwise its impedance will dominate the impedance of the network C_1R_1 and the loop filter will behave as an integrator, yielding an unstable (undamped) loop. Fig. 3 explains the modification of the open and closed loop characteristic brought by C_2 .

As show these plots, without C_2 ($C_2 = 0$) the closed loop characteristics is a low pass filter. When C_2 is added and when its value is low comparing to C_1 , the passband is not affected, but in the rejection band at high frequencies the slope is -40 dB/decade instead of -20 dB/decade. If C_2 is too large ($C_2 = C_1$), the stability of the loop is strongly degraded.

2 Practical design of a PLL

In this document, a choice is made to fix the input specifications of the PLL in the following way:

1. The division coefficient N is fixed by the user
2. The nominal working frequency is fixed by the user. We advise to fix the nominal output frequency to be in the middle of the range of the used VCO. The nominal working frequency is defined by the input reference applied to the PFD. The corresponding output frequency depends on the division factor of the divider.
3. The PLL is designed to work for the nominal frequency. If the PLL needs to work for a range of the frequency, it is up to the user to check the operation of the designed PLL for all frequency range. The developed scripts perform this check for the *full frequency range* of the used VCO. A satisfactory operation of the same PLL in a range of frequencies requires a compromise (e.g., different dynamic behaviour at different frequencies). This compromise should be done by the user, especially if he has specific needs.
4. This generator is designed for a divider with a division factor 24, having intermediate outputs div2, div4, div8. That yields a grid of output frequencies $F_{ref} \times \{2, 4, 8, 24\}$
5. The user may adjust the trend between the the value of the filter capacitors and the current of the charge pump. Since the integrated capacitors may have only limited values (few pF, max. few tens of pF depending on the technology), it may be interesting to reduce the current of the charge pump I_0 , that will yield a reduced value of C_1 and C_2 . However, it will lead to a greater value of R . As a consequence, a compromise is required here, and the last decision is up to the user. Recommended values of I_0 is between 1 and 10 μm .

After performing the design for one selected frequency, the user will have to verify that for other frequencies (corresponding to different VCO gains and hence to different dynamic parameters of the PLL) the dynamic behaviour of the PLL is satisfactory. The dynamic behaviour is mostly defined by the phase margin.

We present now the sequence of step leading to the PLL design.

Step 1. The design of a PLL starts with the design of a VCO, since the output frequency range is the main specification of a PLL. Also, VCO is the most difficult block to design. The choice of the VCO architecture is dictated by several factors related to the purpose of the PLL, to the specification regarding the frequency range and the noise and to the available technology. The solution based on ring CMOS oscillators is the most simple and is often used in the clocking applications. In this project we use the current-starved VCO. However, this PLL design procedure is compatible with any architecture of the VCO.

The VCO is characterised by the characteristic "output frequency versus control voltage". An example of such a characteristic is given in fig. 8a. The derivative of this characteristic provides the link between the VCO gain and the control voltage, yielding a parametric plot "VCO gain versus output frequency", see an example on fig. 8b.

Step 2. Choice of the PLL natural frequency.

The natural frequency of the PLL ω_n defines the bandwidth of the PLL in the phase domain (see an example of fig. 3b). This frequency defines the time duration needed for the PLL to lock, which is of order of $2\pi/\omega_n$.

For the designed PLL, the natural frequency is given by

$$\omega_n = \sqrt{\frac{K_{pfd}G_{vco}}{C_1}}, \quad (6)$$

where K_{pfd} is the gain of the phase-frequency detector and G_{VCO} is the effective gain of the VCO accounting for the frequency division and measured in $rad \cdot Hz/V$:

$$G_{VCO} = 2\pi K_{vco} \cdot \frac{1}{N} \quad (7)$$

The gain of VCO K_{vco} , in Hz/V , is obtained from the "gain-frequency" characteristic of the VCO designed in the step 1, see fig. 8b.

The phase frequency detector gain is given by:

$$K_{PFD} = \frac{I_0}{2\pi} \quad (8)$$

where I_0 is the current generated by the charge pump.

In order to filter out the PWM noise of the phase-frequency detector, the natural frequency should be at least 10 times less than the reference

frequency (the frequency received by the PFD in the lock-in state). Hence, we have

$$\omega_{n \max} = 2\pi f_{ref}/10 \quad (9)$$

In order to fix ω_n , two free independent design parameters are present in (6): I_0 (through K_{PFD}) and C_1 .

We recommend to set I_0 , since it defines the power consumption of the PLL. So, I_0 is an independent input design parameter. Hence, $C_{1 \min}$ is automatically obtained with

$$C_{1 \min} = \frac{I_0 G_{vco}}{\pi \omega_{n \max}^2} \quad (10)$$

We recommend to set C_1 to $C_{1 \min}$, but a larger value may be chosen by the user.

Step 3. Choice of the filter parameters.

We first design the dynamic response of the filter in the passband of the PLL. For that we set $C_2 = 0$ and we choose the remaining parameter, the value of the resistance R . The open loop characteristic is now given by

$$H(p) = K_{pfd} \left(\frac{1}{pC_1} + R \right) \frac{G_{vco}}{p} = \frac{\omega_n^2}{p} \left(\frac{1}{p} + \frac{2\gamma}{\omega_n} \right) \quad (11)$$

where γ is the damping factor of the second-order system.

The input design parameter in this step is the desired phase margin of the PLL open loop response. $PM_{target} = 60$ value is a usual target, since it ensures the fastest transient response. However, at this stage we need to set the phase margin a little bit above the wanted value, since the capacitor C_2 will degrade the stability. Hence, we suggest to add 10° to the target phase margin, setting it to 70° . That corresponds to the the damping factor $\gamma = 0.9$, according to the formula valid for the system with the open loop function given by (12).

$$phase \ margin = \tan^{-1} \frac{2\gamma}{\sqrt{-2\gamma^2 + \sqrt{4\gamma^4 + 1}}} \quad (12)$$

After γ is set, the resistance value is derived:

$$R = \frac{2\gamma}{\omega_n} \quad (13)$$

After fixing R , we can choose the value of C_2 . We will find a maximum value of C_2 degrading the phase margin to the wanted value PM_{target} .

Since the open loop function is now a third order function, we suggest to find C_2 numerically, for instance, by trying for C_2 100 values from 0 to C_1 , or by using any other numeric method of algebraic equation solving.

Step 4. CMOS implementation of the filter. That is explained in the next section.

Setp 5. Validation of the PLL.

The dynamics of the PLL depends on the differential gain of the VCO and on the capacitances of the loop filter. Both of these parameters are function of the voltage V_c at the input of the VCO, whose nominal (average steady-state in locked PLL) defines the output frequency. Since there is a bijective relation between V_c and the output frequency of the VCO f_{vco} , we can speak about the dependence of the VCO gain and of the filter capacitors at the output frequency.

In order to identify the frequency range in which the PLL has an acceptable dynamics (the phase margin and the natural frequency), we recommend to calculate these characteristics for the range of V_c voltages going from 0 to VDD.

3 CMOS implementation of the loop filter

If the used technology offers capacitors, the implementation is straightforward. If not, the capacitors may be implemented with gates of MOS transistors. This section describes implementation of CMOS capacitors of large values.

The greatest capacitance of the MOS transistor is that between the gate and the channel. The drawback of the MOS capacitance is its nonlinearity. Namely, it is much greater in the strong inversion mode than in the sub-threshold mode. Consider a nMOS transistor connected as shown in fig. 4a. Here the equivalent capacitor is between the gate and the ground. In the PLL application, we are mainly interested by the small-signal (differential) capacitance, which is given by the simulator after a DC operating point analysis. This parameter is named C_{gg} .

The maximum value of this capacitance can be estimated as

$$C_{gg\ max} = \epsilon_0 W L / t_{ox}, \quad (14)$$

where t_{ox} is the effective thickness of the gate dielectric, W and L are width and length of the transistor, respectively. A typical relation between the

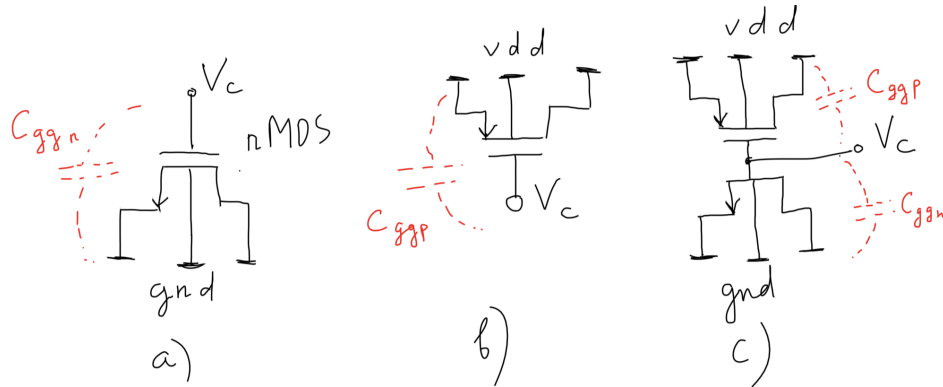


Figure 4: Schematic of MOS capacitors referenced to ground: a) nMOS transistor, b) pMOS transistor, c) complementary MOS capacitor

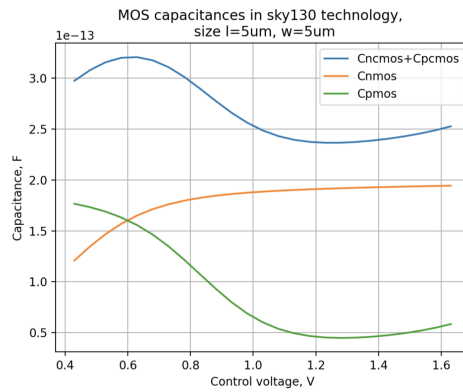


Figure 5: Capacitors of the gate of MOS transistors

gate capacitance and the voltage of a nMOS transistor is shown in fig. 5. The maximum value is only reached when V_{gs} is well above V_{th} . Such a behaviour is generally not satisfactory, since the control voltage needed for the input of the VCO may be below or around V_{th} .

Note that a pMOS transistor may be equally used, as shown in 4b. The corresponding characteristics is given in fig. 5. One can see that for $V_c > V_{dd} - V_{th}$, the capacitance strongly reduced.

For this reason, it is more interesting to use a complementary MOS capacitor composed of NMOS and PMOS transistors of equal size, see fig. 4c. In this case, the ratio between maximum and minimum capacitance value is strongly reduced, passing from 2-3 to 3/2, see fig. 5.

When a capacitance of large value C_t needs to be implemented, the procedure may be the following. One can characterise the capacitance of some unity area transistors, for instance $S_0 = 5\mu m^2$, with $L=W=5\mu m$. That yields a characteristics $C_0(V)$. Since the capacitance is proportional to the area, the required area can be calculated setting $S_0 C_t / C_0(V)$. However, since $C_0(V)$ is not a constant, the designer needs to decide which value from the characteristics $C_0(V)$ will be chosen. That depends on the context. For instance, if the working voltage V is known, the corresponding capacitance value can be chosen as the reference. Otherwise, it can be the minimum or the maximum value of $C_0(V)$, depending on what is less critical for the circuit's characteristics: increase or decrease of the capacitance.

For the PLL, ω_n^2 is inversely proportional to the capacitance C_1 . Since we want ω_n to be *less* than $\omega_{n\max}$, we should take $\min[C_0(V)]$ as the reference. However, the damping factor γ is proportional to $R\omega_n$, and when ω_n decreases, the damping factor decreases as well. That may be bad for the dynamic behaviour of the PLL.

For this reason, it may be reasonable to select basically a *lower* natural frequency ω , design the system for the nominal damping factor at this frequency and select the *maximum value* of $C_0(V)$. In this way, when $C_0(V)$ decreases, the corresponding decrease of ω_n is not critical, and increase of γ yields the dynamic of the system more slow, without causing overshoot.

Alternative strategies may exist. For instance, one can use the average value of $C_0(V)$. Or, another solution can consist in using the voltage range for which the characteristics $C_0(V)$ is constant and maximum, which is in the middle of the V range and hence in the middle of the output VCO frequency range. That corresponds to the maximum of $C_0(V)$. This is possible if the frequency generated by the VCO for this range of the control voltage covers the required output frequencies.

In the designed PLL generator, we select the *maximum* value of $C_0(V_c)$

up	dn	upmos	dnmos
0	0	1	0
0	1	1	1
1	0	0	0
1	1	1	0

Table 1: Truth table for generation of the signals for the charge pump

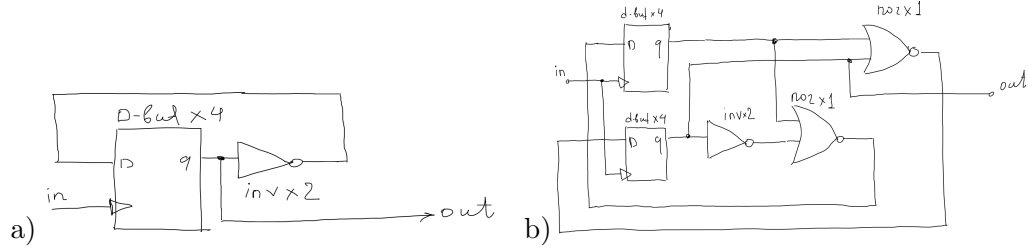


Figure 7: Schematic of dividers by 2 (a) and by 3 (a).

balance the delay of the inverter.

4.2 Divider

The PLL designed in this generator uses a divider with a fixed division factor of 24, with intermediate outputs with division factor 2, 4, 8 and 24. This divider is cascade of three dividers by 2 and one divider by 3.

The schematics of dividers by 2 and by 3 are given in fig. 7.

5 Symmary of the PLL desgin procedure with python generators

1. Design of VCO.

Run the notebook "CMOS_VCO".

Input: maximum desired output frequency.

Output:

- Size of all transistors of the VCO,
- the file "VCO_characteristic.py" containing the characteristics $f_{vco}(Vc)$ and $gain_{vco}(Vc)$ used for the PLL sizing

- the file "CMOS_VCO_cell.cir" containing the netlist of the VCO cell.
2. Design of the charge pump. Run the notebook "chargepump".
- Input parameter: I_{ref} and K , yielding the current I_0 of the charge pump, $I_0 = KI_{ref}$.
- Output:
- the size of all transistors of the chargepump
 - the file "chargepump_cell.cir" containing the netlist of the chargepump cell.
3. Design of the loop filter of the PLL and the assembly of all blocks. Run the notebook "PLL_design".
- Input parameter: the reference (input) frequency of the PLL, f_{ref} and the division factor N .
- Output:
- the nominal values of the filter components (C_1 , C_2 and R), the sizes of the MOS transistors implementing C_1 and C_2 , the netlist "PLL_filter_PI.cell" containing the netlist of the filter.
 - The netlist of the PLL "PLL_cell.cir"
 - The testbench of the PLL, "PLL_testbenchN.cir", where N is the testbench number.

In addition to the generated files, the file "primitives.cir" needs to be present, which indicates the paths toward the PDK models. Also, the netlists of the standard digital cells needs to be available. Here it is provided in the file "StdCellLib_sky130_format.spi".

In summary, the following , the PLL is designed and is ready to be simulated by running the command

```
ngspice PLL_testbench.cir
```

Then, once the netlist is loaded, in the ngspice command environment, it is necessary to write :

```
run
plot <list of the node voltages to display>
```

The testbench file can be modified so to model the PLL under different parameters, for instance, the input frequency.

6 Appendix: Example of a design result

6.1 Case 1

Parameters: VCO: Maximum VCO frequency is $f_{max}=1000$ MHz, the working frequency is 600 MHz (close to the middle of the range). This frequency corresponds to a reference frequency $F_{ref}=25$ MHz and the division factor $N=24$.

For the designed VCO, the gain K_{vco} at F_{ref} is $1.75 \cdot 10^9$ Hz/V.

After running the notebook "CMOS_VCO", the characteristics of the VCO are given in fig. 8.

The evolution of the output frequency is given in fig. 9. The input voltage of the VCO is given in fig. 10. The signals upmos and dnmos (the input of the charge pump) are given in fig. 11. This last plot shows clearly the effect of the parallel-to-ground capacitors at the inputs of the charge pump (dnmos and upmos), which act as low pass filter and modulates the amplitude of short pulses, providing a fine error correction when the PLL is locked.

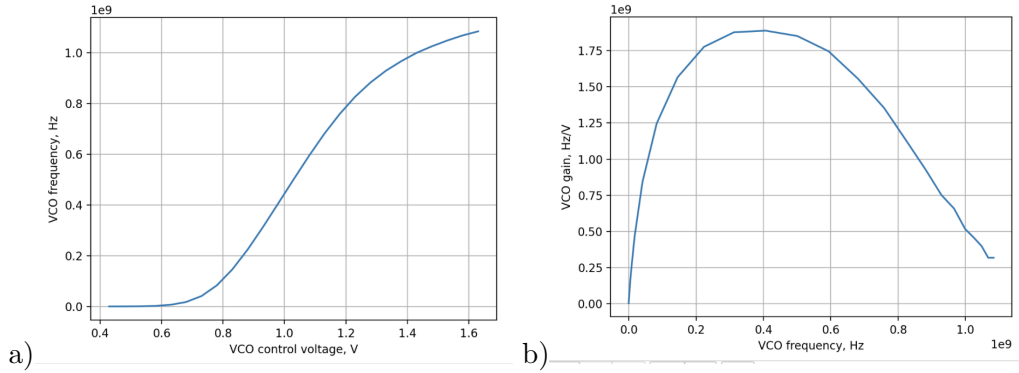


Figure 8: Case 1: characteristics of the designed VCO

PLL: Division factor : $N=24$ $f_{ref}=25$ MHz Targeted phase margin: 60°

Charge pump: $I_{ref}=1 \mu A$, $K=10 \rightarrow I_0=10 \mu A$

Filter parameters : From these parameters, minimum C1 is 2.9 pF. Calculated values of C2: $2.09e-13$ F. Calculated value of R: 38.8 kOhms

Test scenario of the PLL:

A signal signal with frequency $f_{ref} = 25 MHz$ is applied to the input. At the inputs a0a1, the following sequence is generated:

- 11 during 3 microseconds (the transient)

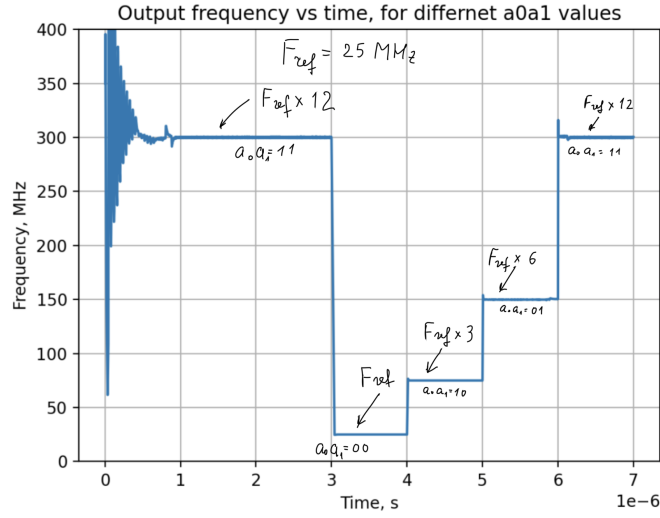


Figure 9: Output frequency obtained from the netlist testbench1.cir.

- sequence 00, 10, 01, 11, 1 microsecond for each combination

The inputs a_0a_1 defining the tapped output of the divider, yielding frequencies $f_{ref} \times \{3, 6, 12\}$ or the copy the reference frequency.

Fig. 10 presents the behaviour of the input voltage of the VCO for 5 simulation cases: $f_{ref} = 10, 15, 20, 25, 30$ MHz. One can see that the lock-in is achieved for all scenario and after each event. The duration of the transient is of order of $1 \mu s$.

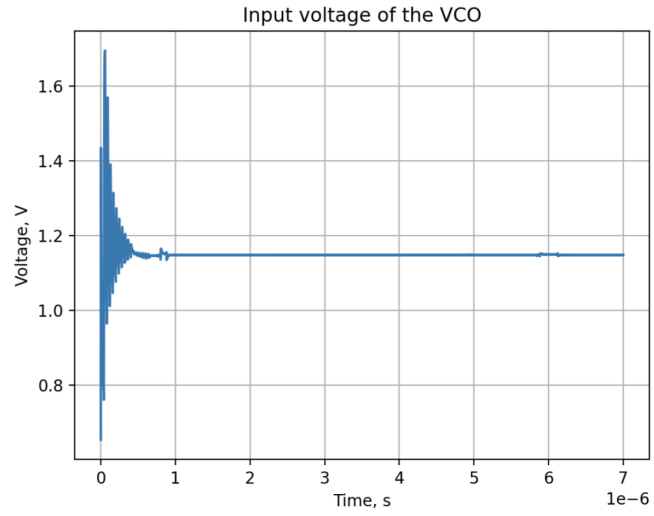


Figure 10: Input voltage of the VCO, test case 1.

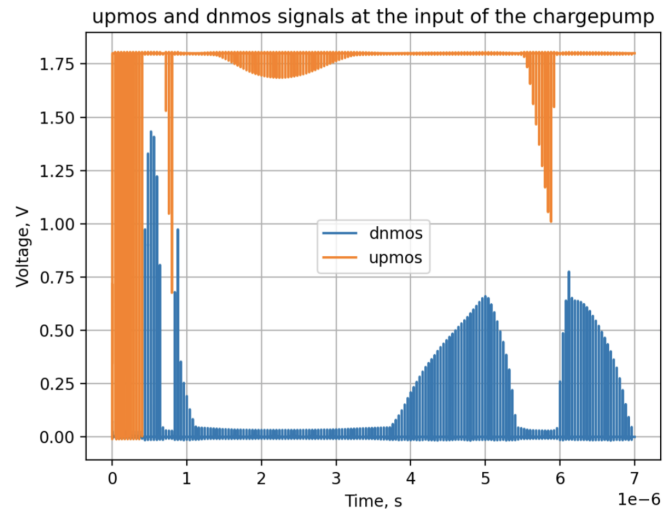


Figure 11: Input voltages of the charge pump, test case 1.